Publications

Whole Brain Emulation - State of the Art

Research Gate

January 17, 2016

Abstract
In the next decade, high performance computing is projected to reach exascale capacity (10^18 floating-point operations per second), a region deemed suitable for emulating one or more continuous learning spiking neuron models of the human brain in realtime [Markram 2012]. Alternatively, specialized hardware may make an exascale computer system unnecessary. Our human...

2 authors

- **Gary Feierbach**
- Randal Koene

Coverage – The Goal of Design Verification

Proceedings of the 2001 Conference on Quality Electronic Design

2001

Investigated a method of checking verification diagnostic coverage using a stuck fault approach. Although compute intensive the approach looked very promising and found diagnostic oversights.

2 authors

- **Gary Feierbach**
- Vijay Gupta

UltraSPARC-I

Proceedings of the 32nd annual ACM/IEEE Design Automation Conference/ACM

January 1995

Paper on the design and verification of the UltraSparc-I processor at Sun Microsystems.

10 authors, including:

- **Gary Feierbach**
- James Gateley
- Miriam Blatt
- Dennis Chen

Forth Tools and Applications

Reston Publishing

1985

Advanced book on the Forth computer language.

2 authors

Gary Feierbach

Paul Thomas

Infotech State of the Art Report (Vol 2): Super-Computers, Infotech International Limited

1979

Paper on the architectural innovations and lessons learned on the Illiac IV project.

2 authors

Gary Feierbach

David Stevenson

The Phoenix Project (Invited Paper)

Infotech State of the Art Super-Computers (Vol 2): Infotech International Limited

1979

This was to be the follow on super-computer to the Illiac IV and this article outlined the architecture of this machine

2 authors

Gary Feierbach

David Stevenson

The Phoenix Array Processor

Seventeenth Annual Technical Symposium/ACM

1978

The Illiac IV processor in the 1970s suggests what capabilities the next generation of large scale array processor should have in the 1980s. The Phoenix array processor presented in this paper is designed to include this experience.

2 authors

Gary Feierbach

David Stevenson

On Processing Element Power in an SIMD Architecture

Proceedings of the 1978 International Conference on Parallel Processing/IEEE Computer Society

1978

This paper examines the trade-offs involved in determining processing element power for a single instruction multiple data stream (SIMD) processor. The serial and parallel capabilities of such a machine are considered in relation to a set of representative sample programs including global weather modeling, computational fluid dynamics, seismic codes and particle codes.